

CLAIMS

What is claimed is:

- 1 1. An integrated circuit (IC) comprising:
2 at least one circuit element;
3 a node coupled to the at least one circuit element;
4 at least one non-floating terminal on a surface of the IC;
5 at least one floating terminal on the surface of the IC; and
6 at least one coupling element to couple any combination of the at least one
7 floating terminal and the at least one non-floating terminal to the node.
- 1 2. The IC recited in claim 1 wherein the node is from the group consisting of power
2 nodes, ground nodes, and input/output nodes.
- 1 3. The IC recited in claim 1 wherein the at least one floating terminal comprises a
2 capacitive element.
- 1 4. The IC recited in claim 3 wherein the capacitive element comprises a connector
2 element, at least one dielectric layer, and a conductor that can be selectively coupled to
3 the node.
- 1 5. The IC recited in claim 4 wherein the connector element comprises a solder
2 bump.
- 1 6. The IC recited in claim 1 wherein the coupling element comprises selector logic
2 coupled to the at least one floating terminal, to the at least one non-floating terminal, and
3 to the node, and comprising at least one control input.

1 7. An integrated circuit (IC) comprising:
2 a plurality of circuit elements;
3 a plurality of nodes coupled to the plurality of circuit elements;
4 a plurality of non-floating terminals on a surface of the IC;
5 at least one floating terminal on the surface of the IC; and
6 selector logic coupled to the terminals and to the plurality of nodes to couple any
7 combination of the at least one floating terminal and one of the plurality of non-floating
8 terminals to one of the plurality of nodes.

1 8. The IC recited in claim 7 wherein the one node is from the group consisting of
2 power nodes, ground nodes, and input/output nodes.

1 9. The IC recited in claim 7 wherein the at least one floating terminal comprises a
2 capacitive element.

1 10. The IC recited in claim 9 wherein the capacitive element comprises a connector
2 element, at least one dielectric layer, and a conductor that can be selectively coupled to
3 the one node.

1 11. The IC recited in claim 10 wherein the connector element comprises a solder
2 bump.

1 12. The IC recited in claim 7 wherein the selector logic comprises at least one control
2 input and further comprises at least one output to selectively couple any combination of
3 the at least one floating terminal and one of the plurality of non-floating terminals to the
4 one node.

1 13. An electronic assembly comprising:
2 an integrated circuit (IC) comprising:
3 at least one circuit element;
4 a node coupled to the at least one circuit element;
5 at least one floating terminal on the surface of the IC; and
6 at least one coupling element to switchably couple the at least one floating
7 terminal to the node; and
8 an IC package substrate comprising a plurality of pads and internal circuit paths,
9 including at least one pad and at least one internal circuit path to couple to the at least
10 one floating terminal.

1 14. The electronic assembly recited in claim 13 wherein the at least one floating
2 terminal comprises a capacitive element, and wherein the capacitive element comprises a
3 connector element coupled to the at least one pad, at least one dielectric layer, and a
4 conductor to be switchably coupled to the node.

1 15. The electronic assembly recited in claim 13 wherein the at least one coupling
2 element comprises selector logic coupled to the at least one floating terminal and to the
3 node, and comprising at least one control input.

1 16. A method of testing an integrated circuit (IC) comprising a plurality of circuit
2 elements and a plurality of terminals including at least one floating terminal, the method
3 comprising:
4 testing the IC;
5 identifying at least one circuit element that is not optimally functioning; and
6 coupling the at least one floating terminal to the at least one circuit element.

1 17. The method recited in claim 16 wherein the IC is from the group consisting of a
2 microprocessor, a microcontroller, a graphics processor, a digital signal processor, an
3 application-specific integrated circuit, a memory circuit, a communications circuit, an
4 artificial intelligence circuit, a neural network, a logic circuit, a computational circuit, a
5 processing circuit, a sensing circuit, a transducer circuit, a power circuit, an amplifying
6 circuit, a data conversion circuit, a data transmission circuit, a data receiving circuit, a
7 custom circuit, and a control circuit.

1 18. The method recited in claim 16 wherein the IC comprises a plurality of floating
2 terminals and selector logic coupled to the plurality of floating terminals, and wherein the
3 method further comprises:
4 providing at least one control signal to the selector logic; and
5 the selector logic coupling at least one floating terminal to the at least one circuit
6 element.

1 19. The method recited in claim 18 wherein the IC further comprises a plurality of
2 non-floating terminals, and wherein the method further comprises:
3 providing at least one control signal to the selector logic; and
4 the selector logic coupling at least one floating terminal and at least one non-
5 floating terminal to the at least one circuit element.

1 20. The method recited in claim 18 wherein the IC further comprises a plurality of
2 non-floating terminals, and wherein the method further comprises:
3 providing at least one control signal to the selector logic; and
4 the selector logic coupling either a floating terminal or a non-floating terminal,
5 but not both, to the at least one circuit element.

1 21. The method recited in claim 16 wherein the IC further comprises a plurality of
2 floating and non-floating terminals, and selector logic coupled to the floating and non-
3 floating terminals, and wherein the method further comprises:
4 providing at least one control signal to the selector logic; and
5 the selector logic coupling any combination of floating and non-floating terminals
6 to the at least one circuit element.

1 22. The method recited in claim 16 wherein the IC comprises at least one floating
2 power terminal, at least one non-floating power terminal, at least one floating ground
3 terminal, at least one non-floating ground terminal, the terminals being coupled to the at
4 least one circuit element, and the IC further comprising selector logic coupled to the
5 terminals, and wherein the method further comprises:
6 providing at least one control signal to the selector logic; and
7 the selector logic coupling any combination of floating and non-floating terminals
8 to the at least one circuit element.

1 23. The method recited in claim 22 wherein the IC further comprises at least one
2 floating input/output (I/O) terminal, and at least one non-floating I/O terminal, the at least
3 one floating I/O terminal and the at least one non-floating I/O terminal being coupled to
4 the at least one circuit element and to the selector logic, and wherein the method further
5 comprises:
6 providing at least one control signal to the selector logic; and
7 the selector logic coupling any combination of floating and non-floating terminals
8 to the at least one circuit element.

1 24. A method of fabricating an integrated circuit (IC) comprising a circuit element
2 and a plurality of non-floating terminals coupled to the circuit element, the method
3 comprising:
4 determining a subset of the plurality of non-floating terminals whose operational
5 characteristics may require adjustment when the IC is operating; and
6 providing a floating terminal for each of the subset of non-floating terminals.

1 25. The method recited in claim 24 wherein the operational characteristics comprise
2 resistive-capacitive (RC) characteristics.

1 26. The method recited in claim 24 wherein at least one of the subset of non-floating
2 terminals is from the group consisting of a power terminal, a ground terminal, and an
3 input/output terminal.

1 27. The method recited in claim 24 and further comprising:
2 providing an IC package substrate comprising a plurality of pads and internal
3 circuit paths, including at least one pad and at least one internal circuit path to couple to
4 each of the floating terminals; and
5 mounting the IC on the IC package substrate.

1 28. The integrated circuit recited in claim 1 wherein the at least one circuit element is
2 selected from the group consisting of a digital logic circuit, an analog circuit, a power
3 circuit, a sense circuit, an amplifier circuit, and a radio circuit.

1 29. The integrated circuit recited in claim 1 wherein the at least one circuit element
2 comprises an inverter circuit.